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Article

A Hybrid Integrated and Low-Cost Multi-Chip Broadband Doherty Power Amplifier Module for 5G Massive MIMO Application

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ABSTRACT

In this paper, a hybrid integrated broadband Doherty power amplifier (DPA) based on a multi-chip module (MCM), whose active devices are fabricated using the gallium nitride (GaN) process and whose passive circuits are fabricated using the gallium arsenide (GaAs) integrated passive devices (IPD) process, is proposed for 5G massive multiple-input multiple-output (MIMO) application. An inverted DPA structure with a low-Q output network is proposed to achieve better bandwidth performance, and a single-driver architecture is adopted for a chip with high gain and small area. The proposed DPA has a bandwidth of 4.4–5.0 GHz that can achieve a saturation of more than 45.0 dBm. The gain compression from 37 dBm to saturation power is less than 4 dB, and the average power-added efficiency (PAE) is 36.3% with an 8.5 dB peak-to-average power ratio (PAPR) in 4.5–5.0 GHz. The measured adjacent channel power ratio (ACPR) is better than −50 dBc after digital predistortion (DPD), exhibiting satisfactory linearity.

1. Introduction

The demand for mobile data rates has undergone substantial growth in recent years, mostly due to the emergence and expansion of various industries. To increase the data rate further, massive multi-input multi-output (MIMO) technology is used in 5G wireless systems. The implementation of massive MIMO has the potential to enhance data rates, expand the coverage of service areas, and improve communication reliability [1]. This enhancement in data rate necessitates the utilization of more intricate modulation techniques and bigger instantaneous signal bandwidths exceeding 100 MHz. It is necessary to configure a separate radio link for each antenna, meaning that the number of radio frequency (RF) power amplifiers (PAs) is equal to that of antennas, with dozens or even hundreds of PAs in a 5G massive MIMO system. Therefore, a massive MIMO transmitter must be compact and small, as it will be deployed in a variety of base stations, both indoors and outdoors. The aforementioned issues will result in an increased need for compact, high-performing, and economically viable RF devices that can be integrated with 64- or even 128-way transmitters. Based on these requirements, a compact structure and miniaturized components hold promise for application in massive MIMO transmitters.

The expected complex and signal-dense scenario gives rise to various problems and challenges, which must be addressed in order to propose effective techniques that ensure the acceptable performance of massive MIMO transmitters, considering energy efficiency and application circuit size. PAs are widely recognized as crucial components in RF transmitters due to their significant power consumption and direct impact on the overall efficiency of RF transmitters. Given the anticipated expansion of signal bandwidth, it is expected that signals exhibiting a high peak-to-average power ratio (PAPR) will be generated. Efficient PAs will be necessary to accommodate the complexity of the modulation methods employed in 5G systems while maintaining high efficiency within the output power back-off (OPBO) range. Several back-off efficient PA architectures have been proposed in the literature, including the Doherty power amplifier (DPA) [2–6], envelope tracking (ET) PA [7], and out-phasing PA [8]. The utilization of ET architecture has proven to be an effective approach for the implementation of energy-efficient transmitters. This architectural solution has gained significant popularity in the context of mobile terminals. However, it is important to note that ET design is not without its limitations, particularly in relation to the bandwidth limitation associated with envelope amplifiers. In the current system, where the commonly used signal bandwidth exceeds 100 MHz, the utilization of ET in massive MIMO transmitters is deemed impracticable. Moreover, in the out-phasing technique, the input signals are separated by two channels with a constant envelope phase modulation, which are respectively passed through the

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high-efficiency PA branch operating in the saturated region and finally synthesized into linearly amplified signals at the output port. However, due to the non-ideal characteristics of actual physical devices and the strict requirement for the phase-matching degree of two PA branches, the out-phasing technique has poor adaptability and is rarely used in the engineering design of base stations. In contrast, the DPA design is quite prevalent in the base stations industry, primarily because of its notable efficiency and comparatively minimal circuit complexity. A DPA consists of two branches with a load modulation between the main and auxiliary amplifiers. The interaction between both branches is facilitated through impedance transformation, whereby the impedances supplied to both branches are dynamically altered based on the envelope magnitude. The main amplifier operates in the low-power region, while the auxiliary amplifier begins to operate when the power exceeds a predetermined power level. DPAs are widely favored in the context of massive MIMO transmitters due to their exceptional performance and straightforward design.

The significant augmentation of RF chains greatly amplifies the scale of a massive MIMO transmitter, resulting in increased system complexity and area size. In the conventional RF chains in a base station, the PAs are implemented on a printed circuit board (PCB), which has the advantage that the components can be replaced flexibly according to the demands of the system. However, the utilization of these designs in a massive MIMO system is hindered by their substantial dimensions. Fortunately, the monolithic microwave integrated circuit (MMIC) displays excellent performance in terms of size for such applications [9–15], achieving the functionality of microwave circuits by linking a series of passive and active components on a chip. In order to create a compact RF transmitter system, the optimal approach is to utilize fully integrated MMICs that are manufactured using a single process. This eliminates the need for external matching components and allows for easy packaging of the chip. The size of MMIC PAs can be greatly reduced compared with that of PAs on a PCB. Nevertheless, the cost of fully integrated MMICs is usually high, due to their large footprints on expensive gallium nitride (GaN) wafers. The GaN process tends to be a favorable choice due to its high power density and exceptional efficiency. despite its high manufacturing cost.

Hybrid integration is an alternative solution to achieve both low-cost and highly integrated PAs [16–18]; it enables a reduction in the size of electronic components through the structure of multi-chip modules (MCMs) while simultaneously enhancing their performance. The packaging methods for MCM assembly are determined by the choice of substrate medium used for attaching the components. A hybrid integrated PA refers to a design in which just the active device power bars are produced using the GaN process, while the matching and biasing circuits are implemented using other cost-effective IPD processes [19,20], which can eliminate the footprint on the PCB. Moreover, the size of a GaN die is reduced to 20% or less of the size of an MMIC die when it is only needed to implement the transistor portion, which can lead to a significant reduction in cost.

To decrease the expenses associated with commercial chips while retaining the advantages of the GaN process, this paper presents a hybrid integrated DPA based on an MCM. The active devices are manufactured using the 0.25 um GaN high electron mobility transistor (HEMT) process from WIN Semiconductors, while all passive circuits are manufactured using WIN Semiconductors' integrated GaAs IPD process, which ensures good dielectric properties and low loss. Various dies are interconnected via bond wires and incorporated into a single package. The mutual coupling effect between adjacent chips and the issue of how to achieve small on-chip inductors and transmission lines are also considered. To meet the requirements of the spectrum mask and distortion, the video bandwidth is optimized by linearization procedures. Finally, these dies are mounted on a four-layer heat-dissipated substrate with a compact package of 10 mm × 6 mm.

This paper is organized as follows. Sections 2 and 3 present the architecture and the specific circuit design of the proposed hybrid DPA, respectively. Section 4 describes the package design in detail. The measurement results are summarized in Section 5, and the conclusion is presented in Section 6.

2. Architecture of the hybrid DPA

2.1. Overall structure of the proposed DPA

The structure of the hybrid DPA based on an MCM is shown in Fig. 1. In the hybrid integration solution, the DPA consists of three parts: the transistors implemented using the GaN process and the input-network and output-network implemented using the GaAs IPD process. The GaAs IPD process is adopted to implement the passive matching networks because it can be integrated with the GaN process in the land grid array (LGA) or quad flat no-leads (QFN) package. In addition, the GaAs IPD process offers more significant performance benefits. The passive devices realized via the GaAs IPD process have a higher Q-value than those obtained via the GaN process, reducing the loss of the matching network and improving the output power and efficiency. Moreover, the GaAs IPD process provides more metal layers to enable the flexible implementation of various passive circuits, such as broadside coupled microstrip lines. Finally, the GaN die of the transistor and the GaAs die of the passive matching network are placed on the same substrate and connected with bonding wires to form a complete chip.

As shown in Fig. 1, to meet the requirement for higher gain, a cascade of two-stage PAs is used. The chip primarily comprises a driver stage and a Doherty stage. As the core part of the chip, the Doherty stage adopts an inverted Doherty architecture based on a low Q-value network to obtain a wide-band active load modulation. The aim of the suggested design technique is to decrease the size of the chip by combining and integrating the design of the input matching networks of the main and auxiliary amplifiers with the power splitter and the output networks of the driver amplifier (DA). The output-matching networks of both the main and auxiliary amplifiers are combined with the output-combining network. The transistors and pad circuits are implemented in the GaN process, while other passive networks are implemented in other processes. A single-driver structure is used for the driver stage to achieve high gain. These techniques are discussed in detail in the following subsections.

2.2. A broadband DPA based on a low Q-value network

In the typical DPA configuration shown in Fig. 2(a), the matching networks of the main and auxiliary amplifiers are developed independently from the input-splitting and output-combining

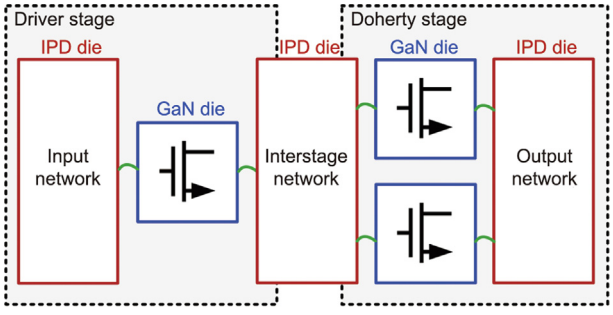

Fig. 1. The architecture of the proposed multi-chip module.

networks. The impedance modulation in the DPA is realized by a $\lambda/4$ transmission line (T-line), which limits the bandwidth performance of the DPA. In this design, an inverted Doherty architecture is adopted to achieve broadband load modulation. As shown in Fig. 2(b), compared with a conventional DPA, two additional $\lambda/4$ T-lines are added in the auxiliary path, which introduce extra resonances for better bandwidth performance of the active load modulation. Two-port Z-parameters, whose ports are the outputs of the main and auxiliary PAs (P_1 and P_2), respectively, are used to describe the increase of the bandwidth in detail. For a conventional DPA, the ***ABCD***-matrix of the $\lambda/4$ T-line can be expressed as follows:

$$\begin{bmatrix} \boldsymbol{A} & \boldsymbol{B} \\ \boldsymbol{C} & \boldsymbol{D} \end{bmatrix} = \begin{bmatrix} \cos\theta & \mathrm{j}R_{\mathrm{opt}}\sin\theta \\ \mathrm{j}\sin\theta/R_{\mathrm{opt}} & \cos\theta \end{bmatrix} \tag{1}$$

where θ represents the phase discrepancy between the main PA and the auxiliary PA, j is the imaginary part, and R_{opt} is the optimal load impedance. The Z-parameters can be derived from Eq. (1):

$$\begin{cases} Z_{11} = \frac{\cos\theta + 2\mathrm{j}\sin\theta}{2\cos\theta + \mathrm{j}\sin\theta} R_{\mathrm{opt}} \\ Z_{22} = \frac{\cos\theta}{2\cos\theta + \mathrm{j}\sin\theta} R_{\mathrm{opt}} \\ Z_{12} = Z_{21} = \frac{1}{2\cos\theta + \mathrm{j}\sin\theta} R_{\mathrm{opt}} \end{cases} \tag{2}$$

The relationship between the fundamental voltage (V_{m}, V_{a}) and the fundamental current (I_{m}, I_{a}) of the main amplifier and the auxiliary amplifier can be expressed as Eq. (3) based on the Z-parameters:

$$\begin{cases} V_{\mathrm{m}} = Z_{11}I_{\mathrm{m}} + Z_{12}I_{\mathrm{a}} \\ V_{\mathrm{a}} = Z_{21}I_{\mathrm{m}} + Z_{22}I_{\mathrm{a}} \end{cases} \tag{3}$$

Given that the input voltage and the saturated input voltage of the transistor are V_{in} and $V_{\mathrm{in,max}}$, respectively, the normalized input voltage α can be expressed as follows:

$$\alpha = V_{\mathrm{in}}/V_{\mathrm{in,max}} \tag{4}$$

The saturated amplitude of the fundamental current of the transistor is $I_{\mathrm{max}}/2$, and the main and the auxiliary amplifier current based on the normalized input voltage α are:

$$I_{\mathrm{m}} = \alpha(I_{\mathrm{max}}/2) \tag{5}$$

$$I_{\mathrm{a}} = \begin{cases} 0 \; 0 \le \alpha < 0.5 \\ (\alpha - 0.5)I_{\mathrm{max}}\mathrm{e}^{-\mathrm{j}\theta} \; 0.5 \le \alpha < 1.0 \end{cases} \tag{6}$$

where $e^{-\mathrm{j}\theta}$ indicates that the auxiliary PA current is in phase ahead of the main PA current θ. Substituting Eqs. (2), (5), and (6) into Eq. (3), the fundamental voltage of the main and auxiliary amplifiers can be expressed clearly. Then, the expression of drain efficiency (DE) can be calculated. The DE curves of the conventional DPA at different frequencies are presented in Fig. 3(a). It is clear that the back-off efficiency drops significantly when the operating frequency deviates from the central frequency. As a result, it is difficult to realize a broadband DPA based on the conventional structure [21].

The proposed inverted Doherty architecture based on a low-Q output network improves the common load R_{L} (load impedance) to R_{opt} (optimal load impedance). The characteristic impedance of the T-line after the main amplifier is increased to $\sqrt{2}R_{\mathrm{opt}}$, and two $\lambda/4$ T-lines whose characteristic impedances are $\sqrt{2}R_{\mathrm{opt}}$ and R_{opt} are introduced after the auxiliary amplifier. Compared with a conventional DPA, the proposed architecture has an impedance conversion ratio of two in both the saturation and back-off regions, which will expand the bandwidth significantly. The transmission matrix of the $\lambda/4$ T-line after the main amplifier can be expressed as follows:

$$\begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} = \begin{bmatrix} \cos\theta & \mathrm{j}\sqrt{2}R_{\mathrm{opt}}\sin\theta \\ \mathrm{j}\sin\theta/(\sqrt{2}R_{\mathrm{opt}}) & \cos\theta \end{bmatrix} \tag{7}$$

The transmission matrix of the two cascaded $\lambda/4$ T-lines after the auxiliary amplifier can be written as follows:

$$\begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix} = \begin{bmatrix} \frac{(\sqrt{2}+1)\cos(2\theta)+\sqrt{2}-1}{2\sqrt{2}} & \mathrm{j}\frac{(\sqrt{2}+1)R_{\mathrm{opt}}\sin(2\theta)}{2} \\ \mathrm{j}\frac{(\sqrt{2}+1)R_{\mathrm{opt}}\sin(2\theta)}{2\sqrt{2}R_{\mathrm{opt}}} & \frac{(\sqrt{2}+1)\cos(2\theta)-\sqrt{2}+1}{2} \end{bmatrix} \tag{8}$$

According to Eqs. (7) and (8), the Z-parameters can be expressed as follows:

$$\begin{cases} Z_{11} = \frac{A_1D_2R_{\mathrm{opt}} + B_1(D_2 + C_2R_{\mathrm{opt}})}{C_1D_2R_{\mathrm{opt}} + D_1(D_2 + C_2R_{\mathrm{opt}})} \\ Z_{22} = \frac{A_2D_1R_{\mathrm{opt}} + B_2(D_1 + C_1R_{\mathrm{opt}})}{C_2D_1R_{\mathrm{opt}} + D_2(D_1 + C_1R_{\mathrm{opt}})} \\ Z_{12} = Z_{21} = \frac{R_{\mathrm{opt}}}{C_2D_1R_{\mathrm{opt}} + D_2(D_1 + C_1R_{\mathrm{opt}})} \end{cases} \tag{9}$$

The main amplifier will saturate when $\alpha < 0.5$ with the low-Q output network, which results in the main PA working in an overexcited state or even burning out. Therefore, the main and auxiliary amplifier currents of the proposed low-Q inverted DPA are expressed as follows:

$$I_{\mathrm{m}} = \alpha(I_{\mathrm{max}}/2) \tag{10}$$

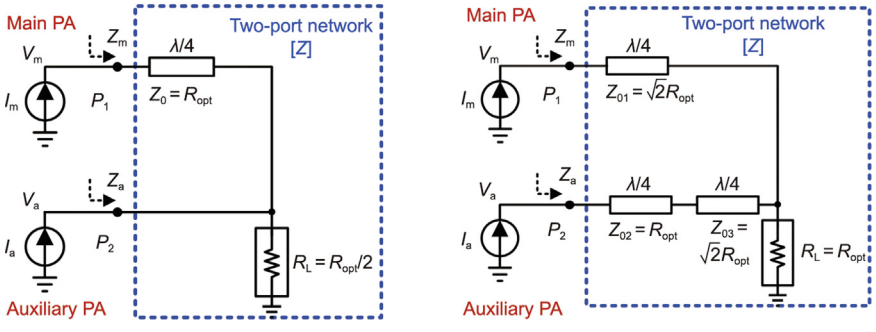

Fig. 2. The architecture of (a) a conventional DPA and (b) the inverted DPA. V_{m}: the fundamental voltage of the main amplifier; V_{a}: the fundamental voltage of the auxiliary amplifier; I_{m}: the fundamental current of the main amplifier; I_{a}: the fundamental current of the auxiliary amplifier; Z_{m}: the impedance of the main PA; Z_{a}: the impedance of the auxiliary PA; Z_0, Z_{01-03}: the characteristic impedance of the corresponding T-lines; λ: the wavelength; R_{opt}: the optimal load impedance; R_{L}: the load impedance; P_1, P_2: the input nodes of the main PA and the auxiliary PA.

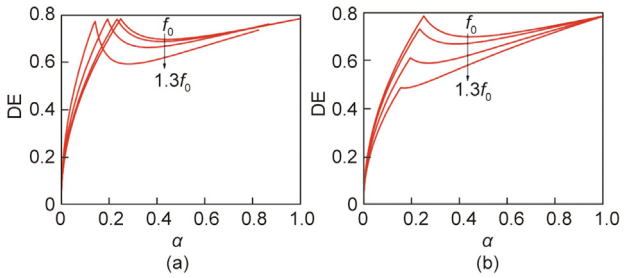

Fig. 3. The DE curves of (a) a conventional DPA and (b) an inverted DPA. f_0: the center frequency.

$$I_a = \begin{cases} 0\ 0 \le \alpha < \tau \\ \frac{\alpha-\tau}{1-\tau} I_{max} e^{-j\theta} \tau \le \alpha < 1 \end{cases} \quad (11)$$

where τ indicates the normalized input voltage when the main PA first reaches saturation.

The DE is calculated and shown in Fig. 3(b), similarly to the conventional DPA. Compared with Fig. 3(a), the back-off efficiency at the non-central frequency is significantly improved, but the saturation power efficiency is decreased because the impedance conversion ratio of the low-Q network in the saturation region is not 1. Since the DPA works in the back-off region most of the time in actual applications, the proposed low-Q structure can expand the bandwidth of the DPA.

2.3. Architecture of the driver stage

The implementation of Doherty technology in the cascade circuit can be derived from three different structures due to the different driver stages, as shown in Fig. 4. The addition of the driver stage will increase the direct current (DC) power consumption and deteriorate the overall efficiency, but the deterioration of efficiency is different under different drive structures. Fig. 5 shows the overall efficiency curves of the two drive structures under different final-stage gains when assuming that all PAs work in the ideal class-B state, with constant gain, and different stages are isolated from each other. It can be seen that the saturation efficiency of the Doherty-driver structure and that of the single-driver structure are the same, but the back-off efficiency of the Doherty-driver structure is always higher; moreover, the lower the final-stage gain, the more obvious the advantage of the Doherty-driver structure in terms of back-off efficiency. However, considering the non-ideal factors in the actual design, this conclusion is not reasonable. To ensure a reasonable time sequence of conduction, the auxiliary PA in the DPA is usually biased in the class-C state, which will reduce the gain in the saturation zone. The input network of the DPA requires a power splitter, which will introduce at least 3 dB of gain loss in the OPBO region, so that the overall gain of the Doherty-driver structure is the lowest. In addition, if the driver stage also uses the Doherty structure, the linearity will further deteriorate, increasing the difficulty of digital predistortion (DPD). Due to the disadvantage of gain and linearity, the Doherty-driver structure is rarely used in actual products.

For the dual-driver structure, the DA before the auxiliary PA is biased in the class-C state and does not work in the back-off region. Obviously, the DA in the single-driver structure needs to provide more power in the back-off region, so the DC power consumption is higher, resulting in a lower overall back-off efficiency. Fig. 6 gives the 6 dB back-off efficiency of a single-driver structure and a dual-driver structure with different final-stage gains. As shown in Fig. 6, the efficiency of the dual-driver structure is always higher than that of the single-driver structure. However, the dual-driver structure is commonly used in the millimeter wave band due to the low gain of single-stage amplifiers [22]. The efficiency advantage of a dual-driver is not obvious, and the chip area is large at low frequencies (sub-6 GHz). Thus, a single-driver structure is adopted in the proposed design [23]. The output matching network of the single-driver PA and the input network of the DPA can be combined into an interstage matching network. Therefore, the two-stage cascade hybrid integration solution is composed of five parts.

3. Circuit design

3.1. GaN transistor

In the early stage of circuit design, the gate width of the transistor can be optimized according to the target output power. The main and auxiliary amplifiers of the DPA should be designed to have an optimal load impedance of 100 Ω, and a post matching network should be applied using a simple inductor–capacitor (LC) network after the combining node, so that the main amplifier and auxiliary amplifier of the DPA are designed to have an optimal load impedance of 100 Ω. When the two amplifiers are combined, they can be directly connected to a 50 Ω load without the need for a matching network. Because the parasitic capacitance is related to the gate width of the transistor, it is also necessary to consider the absorption of the resonant inductance in subsequent matching network design when optimizing the gate width.

In the final stage of the DPA, two GaN transistors with a 4:5 gate width ratio are used to implement an asymmetric Doherty circuit in order to increase the back-off efficiency to meet the high PAPR requirements in 5G communication. Two discrete GaN transistors can not only improve the isolation between the main and auxiliary circuits but also make the subsequent package design more flexible. When the distance between GaN transistors is greater, the heat that must be transferred through the substrate will be faster and more dispersed. According to the power level demand, the gate widths of the DPA's main and auxiliary transistors are $2 \times 10 \times 200$ μm and $2 \times 10 \times 250$ μm, respectively, and the gate width of the driver stage transistors is 8×200 μm. The optimal load impedances of the $2 \times 10 \times 200$ μm, $2 \times 10 \times 250$ μm, and 8×200 μm transistors are 20, 14, and 66 Ω, respectively.

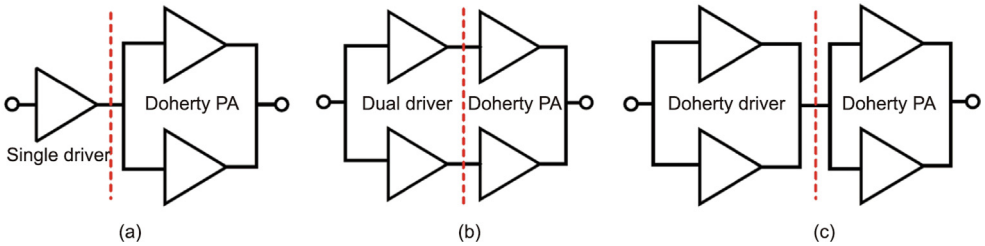

Fig. 4. The architecture of (a) a single driver, (b) a dual driver, and (c) a Dohertydriver.

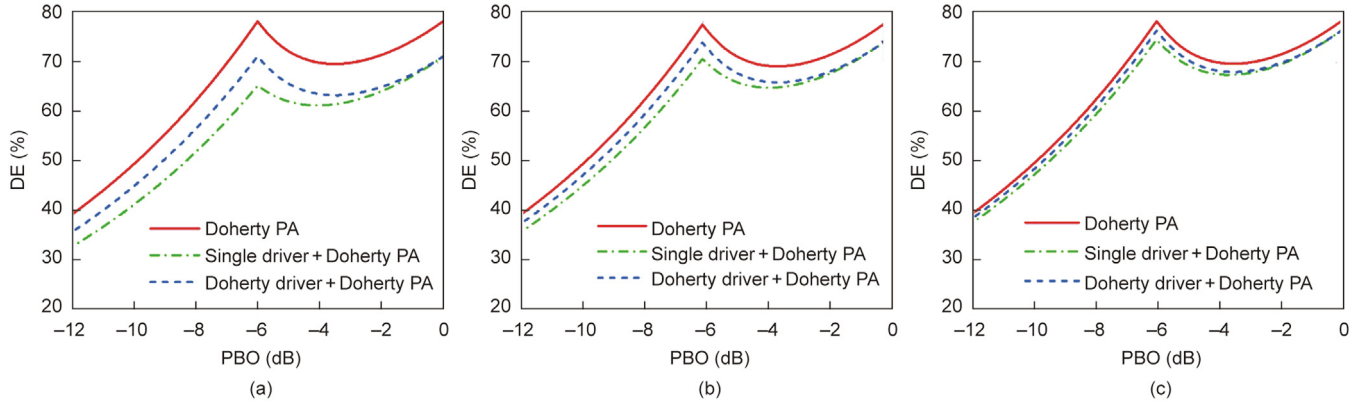

Fig. 5. The DE curves under different final-stage gains. (a) 10 dB; (b) 13 dB; (c) 16 dB. PBO: power back-off.

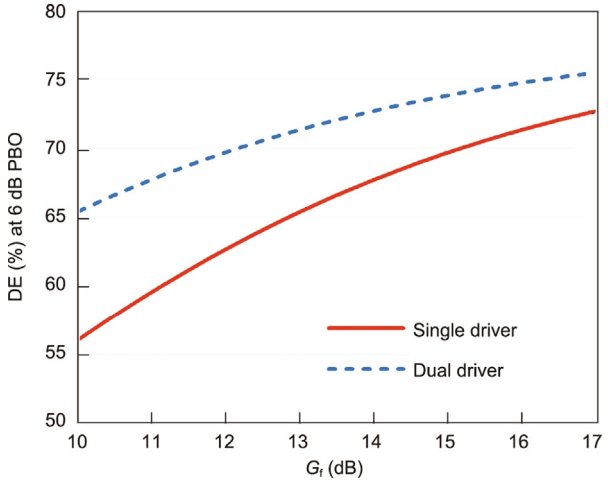

Fig. 6. The 6 dB back-off efficiency of a single-driver and dual-driver structure. G_f: the gain of the final stage.

3.2. Matching network of the final DPA

The design of the matching network includes the input and output network. The low-Q output matching network of the DPA consists of three $\lambda/4$ T-lines. The implementation of lumped parameter circuits is discussed first for the convenience of analysis; all inductors in the matching networks of the proposed hybrid PA are realized with T-lines to reduce the loss.

The $\lambda/4$ T-line can be replaced with a high-pass or low-pass lumped parameter π-type network, as shown in Fig. 7. The parameters of the π-type network can be expressed as follows:

$$\begin{cases} L_T = Z_T/(2\pi f_0) \\ C_T = 1/(2\pi f_0 Z_T) \end{cases} \tag{12}$$

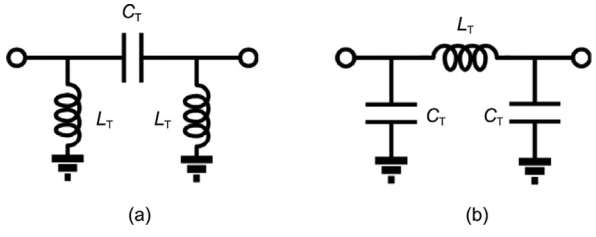

Fig. 7. Lumped parameter $\lambda/4$ T-line. (a) High-pass structure; (b) low-pass structure. C_T: the capacitor of the π-network; L_T: the inductor of the π-network.

where Z_T is the characteristic impedance, f_0 represents the center frequency, C_T is the capacitor of the π-type network and L_T is the inductor of the π-type network. The shunt inductor in the high-pass network can be used for the voltage supply, and the series capacitor can be used to isolate the direct currents; however, the high-pass network cannot absorb the output capacitance of the transistor, which limits the working bandwidth of the DPA. For the low-pass network, the shunt capacitor can absorb the parasitic capacitance of the transistor, so it has better bandwidth performance in the actual design, but the low-pass network cannot supply the drain voltage directly and isolate the DC currents; thus, it is necessary to adopt an additional bias circuit in the output network of the main amplifier. According to Eq. (12), C_T gradually decreases as the frequency increases, and the output parasitic capacitance of the transistor (C_{out}) will exceed C_T. Therefore, the introduction of an additional shunt inductor is needed to neutralize C_{out}, as shown in Fig. 8(a). The inductor L_p in Fig. 8(a) can be deduced as follows:

$$L_p = \frac{1}{(2\pi f_0)^2 (C_{out} - C_T)} \tag{13}$$

However, the L_p will be large and difficult to implement in the actual circuit due to the small $C_{out} - C_T$. To tackle this issue, the C_T in Fig. 8(a) can be replaced by $L_p//C_{out}$, as shown in Fig. 8(b); then, the π-type inductor network in Fig. 8(b) can be converted into a T-type inductor network, as shown in Fig. 8(c). The inductor in the T-type network can be deduced as follows:

$$\begin{cases} L_{T1} = L_T/(2 + L_T/L_P) \\ L_{T2} = L_P/(2 + L_T/L_P) \end{cases} \tag{14}$$

The inductor value of the T-type network is reduced by half from Eq. (12). The shunt inductor L_{T2} can be used for the drain voltage supply, but an additional isolation capacitor is still required. The T-type output network of the main PA was simulated, and the result is presented in Fig. 9(a). The simulation shows that the S_{11} of the proposed output network is better than −10 dB and the loss is less than 0.9 dB within the range of 4.3–5.5 GHz.

The two $\lambda/4$ T-lines after the auxiliary amplifier can be implemented with a low-pass lumped structure, as shown in Fig. 10(a), which exhibits a −180° phase shift at the center frequency. Fig. 10(b) shows the actual circuit of the output network after the auxiliary amplifier. The capacitance C_T is a combination of C_{T1} and C_{T2}, and the shunt C_{T1} near the transistor absorbs the output parasitic capacitance of the transistor. An additional shunt inductor L_p is added to neutralize C_{out} and supply the DC voltage at the same time. Fig. 9(b) shows the *S*-parameter simulation of the auxiliary amplifier's output network. The proposed matching

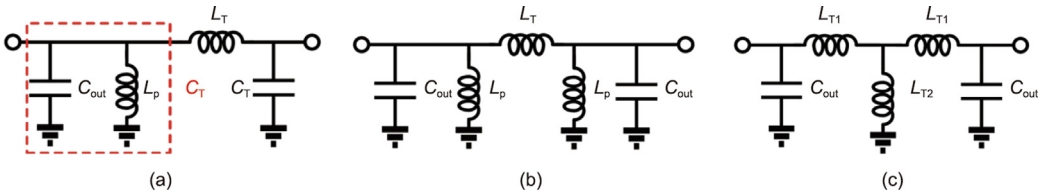

Fig. 8. The absorption of the transistor's output capacitor: (a) shunt inductor, (b) π-type inductor network, and (c) T-type inductor network. C_{out}: the output parasitic capacitance of the transistor; L_p, L_{T1}, and L_{T2}:the inductors of the matching networks.

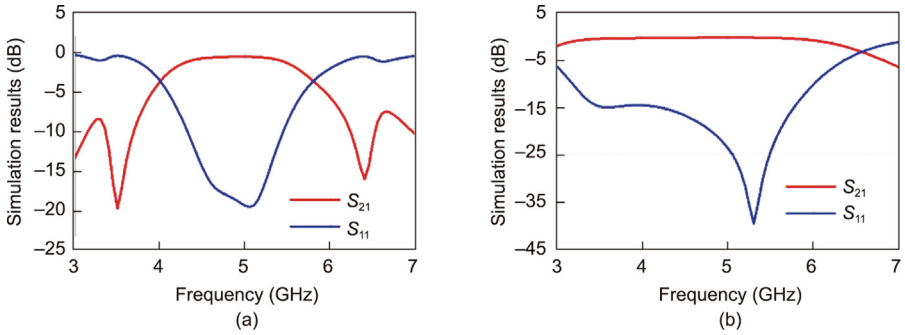

Fig. 9. Simulation results of the output matching network: (a) main PA and (b) auxiliary PA.

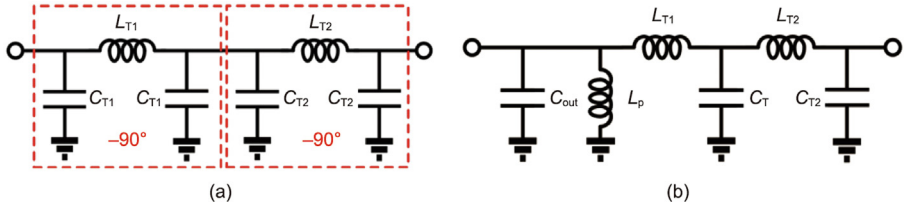

Fig. 10. The lumped parameter output network of the auxiliary amplifier: (a) the low-pass lumped structure and (b) the actual circuit. C_{T1} and C_{T2}: the capacitors of the output network.

network has excellent S_{11} results with low insertion loss over a wide bandwidth.

The input network of the final DPA unifies the concurrent design of the power splitter. The input matching of the main amplifier adopts a band-pass structure, while the input network of the auxiliary amplifier uses a two-stage low-pass LC structure. Due to the influence of the parasitic feedback capacitance in the transistors, the load impedance has an impact on the input matching. Therefore, when designing the input-matching network of the main amplifier, it is imperative to balance the matching effect of the back-off and saturation regions. A high-pass lumped parameter Wilkinson power splitter is utilized as the input power splitter of the DPA. A traditional lumped parameter Wilkinson power splitter is generally based on a π-type or T-type network, which has the issues of high loss and a narrow bandwidth. Therefore, the proposed design uses the LC-ladder structure of the Wilkinson power splitter to achieve low loss and a wide bandwidth.

3.3. Matching network of the driver amplifier

The output network of the DA is co-designed with the power splitter of the final DPA to reduce the chip area. A T-type inductor network is used as the output matching network of the driver stage; it can absorb the output capacitance of the transistor and is equivalent to a T-line over a wide frequency band for low loss. When designing the output matching network of the driver stage, the load impedance must be based on the input impedance of the final DPA in the saturation region because the input impedance of the final DPA changes with the output power.

The input matching network of the DA uses a two-stage LC bandpass network with a 3 Ω resistor to improve stability. In addition, the bias of the driver stage is in the deeper class-AB state, leading to an expansion of the gain curve, which effectively compensates for the gain compression of the final DPA. As a result, the overall hybrid PA demonstrates better linearization.

4. Packaging design

In hybrid integration, the GaN die of the transistors and the IPD die of the passive matching network are placed on a substrate and connected with bond wires. The design of the bond wire must consider not only the current tolerance of the transistors but also the influence of the wire's own parasitic parameters on the passive matching network in different frequency ranges. Both ends of the bond wire are respectively connected to the pad of the GaN transistor and the pad of the IPD die or the pins of the substrate. The height difference at both ends and the change in the curvature of the bond wire caused by different chip thicknesses will cause various parasitic parameter values. Therefore, the design of the bond wire must be taken into consideration in the design of the passive matching network. In the design of the GaN transistor, the output capacitance of the transistor must be neutralized at the drain terminal. The equivalent inductance provided by the bond wire can form an LC network with the intrinsic output capacitance of the transistor to

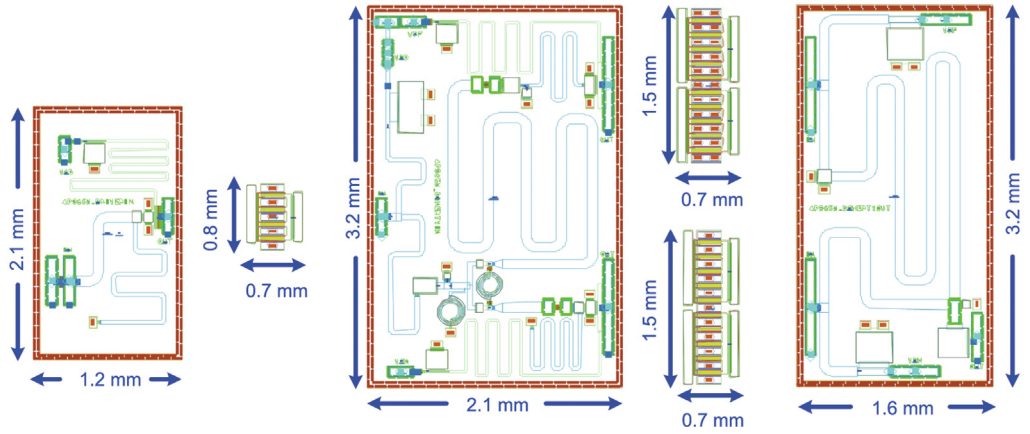

Fig. 11. Layout of the proposed hybrid integrated DPA.

achieve neutralization. It is difficult to ensure that the shape of each bond wire is completely consistent in the bonding process. To address this issue, the parallel connection of multiple bond wires can reduce the influence of the differences between different bond wires on the equivalent inductance. After electromagnetic (EM) simulation, the bond wires used to link the transistors can be placed at the edge of the passive matching network in order to undertake impedance matching. The RF input and RF output ports both use three bond wires, whose equivalent characteristic impedance is close to 50 Ω; and, they have little influence on the matching.

Fig. 11 shows the layout of the single-driver Doherty amplifier, which consists of six dies including the driver input matching circuit, driver transistor, driver output matching circuit, input and output network of the final DPA, and main and auxiliary amplifier transistors. Complete circuits of the implemented DPA were EM-simulated using ADS software from Keysight (USA). The full module is packaged in a 10 mm × 6 mm LGA. All six dies are placed on the four-layer substrate, as shown in Fig. 12, and fixed with conductive silver adhesive. Because the heat dissipation of a GaN die is very high, copper is embedded in the substrate under each GaN die to prevent the transistor from overheating.

The three-dimensional (3D) structure of the package simulated in the high-frequency simulator structure (HFSS) is shown in Fig. 13(a). Fig. 13(b) presents the frequency response of the bond wires at the RF input and RF output ports. The simulation results for the S_{11} are better than −24 dB within 4.4–5.0 GHz.

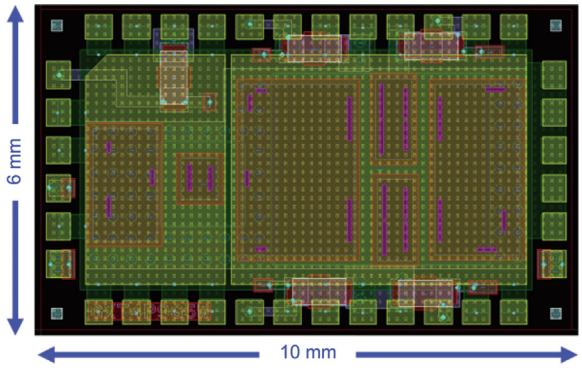

Fig. 12. Layout of the substrate.

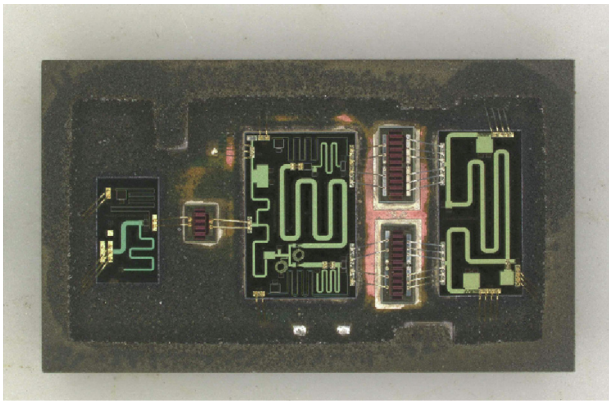

Fig. 14. A photograph of the fabricated hybrid integrated DPA.

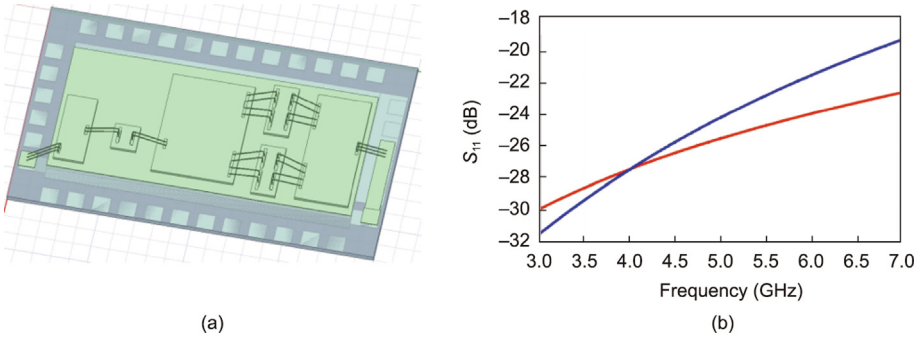

Fig. 13. (a) HFSS simulation model of the entire package; (b) simulation results of bond wires at the RF input port and RF output port.

5. Measurement results

The proposed fabricated hybrid integrated DPA is shown in Fig. 14. It was tested under the following bias: a drain voltage of 28 V; static circuits of the main amplifier and driver stage of 72 and 30 mA, respectively; and a gate voltage of the auxiliary amplifier of 3.4 V. The measured S-parameters are presented in Fig. 15 (a). The measured small-signal gain is higher than 30 dB, and the S_{11} is better than −7 dB at a range of 4.8–5.0 GHz.

Fig. 15(b) shows the large-signal measurement results under a pulsed signal with a 10% duty signal. The duty cycle of the pulse is 20 μs/200 μs. It can be seen that the saturation power within 4.4–5.0 GHz is better than 45 dBm, and the gain compression from 37 dBm to saturation power is less than 4 dB. Moreover, the gain characteristics at different frequencies are consistent, which reduces the difficulty of the broadband DPD correction.

For the modulation measurements presented in Fig. 16(a), 100 MHz LTE signals with a 8.5 dB PAPR are generated by the vector signal source (SMW200A, Rohde & Schwarz, Germany), and the output signals are demodulated using a Rohde & Schwarz (USA) FSW43 device. The adjacent channel power ratio (ACPR) and power-added efficiency (PAE) results are summarized in Fig. 16 (b). The average PAE is 36.3% with an 8.5 dB PAPR in 4.5–5.0 GHz. To further demonstrate the linearity of the proposed PA, an ACPR with a generalized memory polynomial (GMP) DPD algorithm is also shown in Fig. 16(b). The ACPR is better than −50 dBc after DPD in the working band. Fig. 16(c) presents the output power spectrum density (PSD) at 4.9 GHz. The ACPR with and

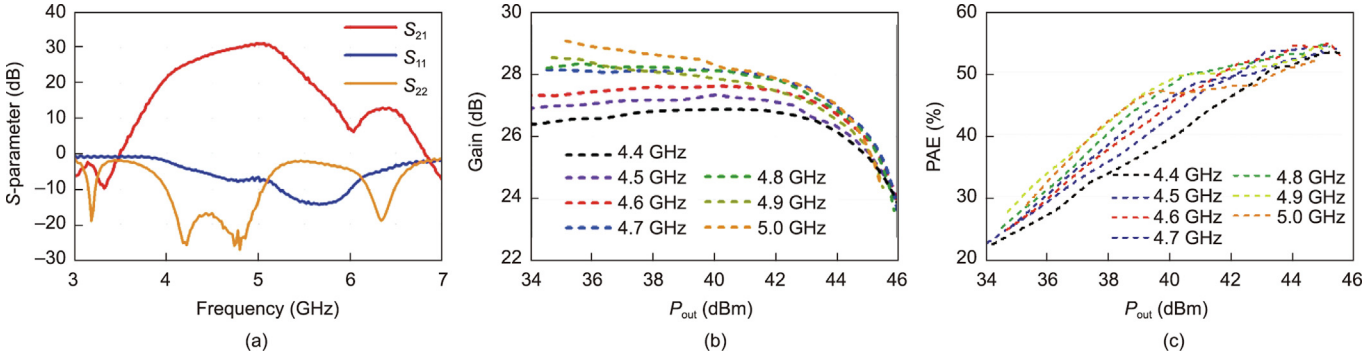

Fig. 15. (a) The measured *S*-parameters, (b) large-signal measurement results for gain versus P_{out}, and (c) large-signal measurement results for power-added efficiency (PAE) versus P_{out}. P_{out}: the output power.

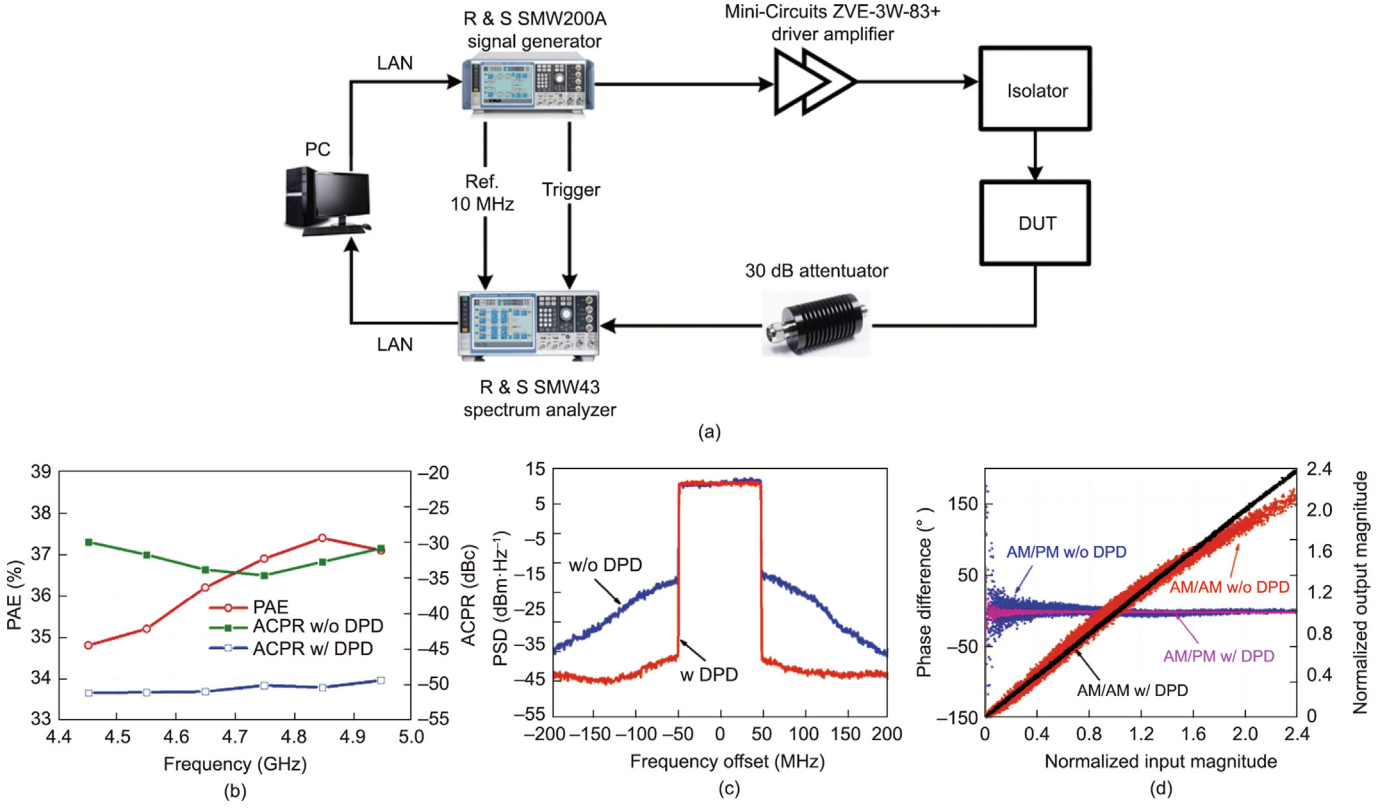

Fig. 16. (a) The setup, (b) the result of the modulation measurement, and (c) output power spectrum density. (d) AM–AM and AM–PM characteristics. PC: personal computer; LAN: local area network; DUT: device under test; Ref: reference signals; ACPR: adjacent channel power ratio; PSD: power spectrum density; w/: with; w/o: without; AM: amplitude modulation; PM: phase modulation.

Table 1
Comparison with other GaN DPAs.

Date	Frequency (GHz)	P_{sat} (dBm)	DE at saturation (%)	DE at PBO (%)	PBO (dB)	Gain at PBO (dB)	Chip area of GaN (mm × mm)	Technology
2015 [5]	1.8	42.8	N/A	57.2	6.0	18.8	3.09 × 2.23	MMIC
2015 [24]	2.1–2.7	40.0–4.01	N/A	48.0–62.0	7.6	12.0–14.0	2.65 × 1.90[a]	MMIC
2018 [18]	5.9	38.7	47.3	49.5	6.0	14.4	2.49 × 1.56	MMIC
2018 [18]	5.1–5.9	36.0–38.7	N/A	32.0–5.01	6.0	14.4–17.3	2.50 × 1.60	MMIC
2019 [25]	4.5–5.2	40.4–41.2	55.0–63.0	47.0–50.0	6.0	8.0–11.0	2.20 × 2.10	MMIC
2019 [26]	4.5–6.0	35.0–36.0	43.0–49.0	24.0–32.0	6.0	7.6–11.6	3.00 × 2.80	MMIC
2021 [27]	4.6–5.2	41.8–42.1	63.8–68.4	53.3–57.4	6.0	12.8	2.50 × 2.45	MMIC
2022 [28]	4.1–5.6	38.4–39.5	51.7–60.8	38.4–39.5	6.0	8.3–11.2	2.60 × 3.00	MMIC
This work	4.5–5.0	45.7–46.3	56.0–60.0	35.0–37.5	8.5	27.0–28.2	3.80 × 0.70[b]	MCM

P_{sat}: the saturated output power; DE: drain efficiency; PBO: power back-off.
[a] The partial output network is off-chip.
[b] Two GaN chips of 1.5 mm × 0.7 mm and one GaN chip of 0.8 mm × 0.7 mm were used in this work.

without DPD is −31.47/−30.07 dBc and −52.15/−51.88 dBc, respectively. According to these results, the proposed DPA presents satisfactory linearity.

Table 1 shows the performance of the proposed DPA and provides a comparison with other GaN DPAs. It can be seen that the proposed DPA achieves the largest saturated output power and gain at power back-off (PBO). Before this work, a relatively small chip area of 2.5 mm × 1.6 mm was realized by the MMIC in Ref. [18]. However, as mentioned above, MCM technology means that only active device power bars are manufactured using the GaN process. Therefore, the compact GaN chip area results in a very low cost. The proposed DPA is well-suited for 5G massive MIMO base stations and other broadband wireless communication systems due to its advantageous bandwidth and application circuit size.

6. Conclusions

In this research, a hybrid integrated broadband DPA based on an MCM was designed for 5G massive MIMO application. The active devices of the proposed DPA are fabricated using the GaN process, while all passive circuits are fabricated using the GaAs IPD process with a high dielectric and low loss. An inverted DPA structure with a low-Q output network was proposed to broaden the bandwidth, and a single-driver architecture was adopted for high gain and a small chip area. The measured results showed that the working bandwidth is over 500 MHz and the saturation power in 4.4–5.0 GHz is better than 45 dBm. The modulation measurement demonstrated that the average PAE is 36.3% with an 8.5 dB PAPR in 4.5–5.0 GHz, and the ACPR is better than −50 dBc after applying DPD.

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Compliance with ethics guidelines

Fei Huang, Guansheng Lv, Huibo Wu, Wenhua Chen, and Zhenghe Feng declare that they have no conflict of interest or financial conflicts to disclose.

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